

Fig. 1

FIG. 2 is a block diagram of a system 200 for wafer processing. The system 200 includes a wafer source 210, an RTA process chamber 220, an  $R_s$  measurement chamber 230, a feedback generator 250, a data store 260, and a wafer destination 240. The wafer source 210 is connected to the RTA process chamber 220. The RTA process chamber 220 is connected to the  $R_s$  measurement chamber 230. The  $R_s$  measurement chamber 230 is connected to the wafer destination 240. The RTA process chamber 220 is also connected to the feedback generator 250. The feedback generator 250 is connected to the data store 260. The data store 260 is connected to the wafer source 210.

200

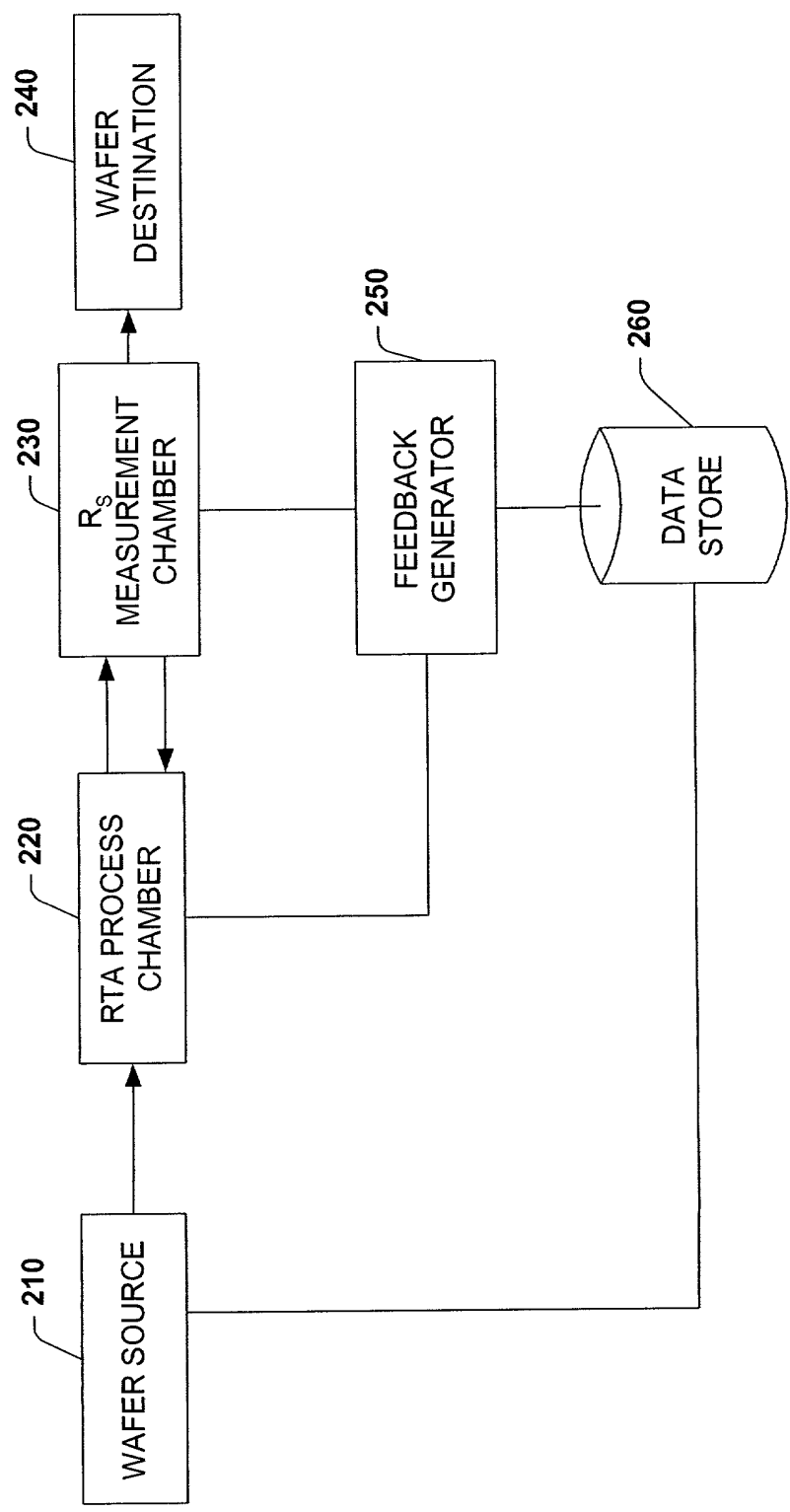
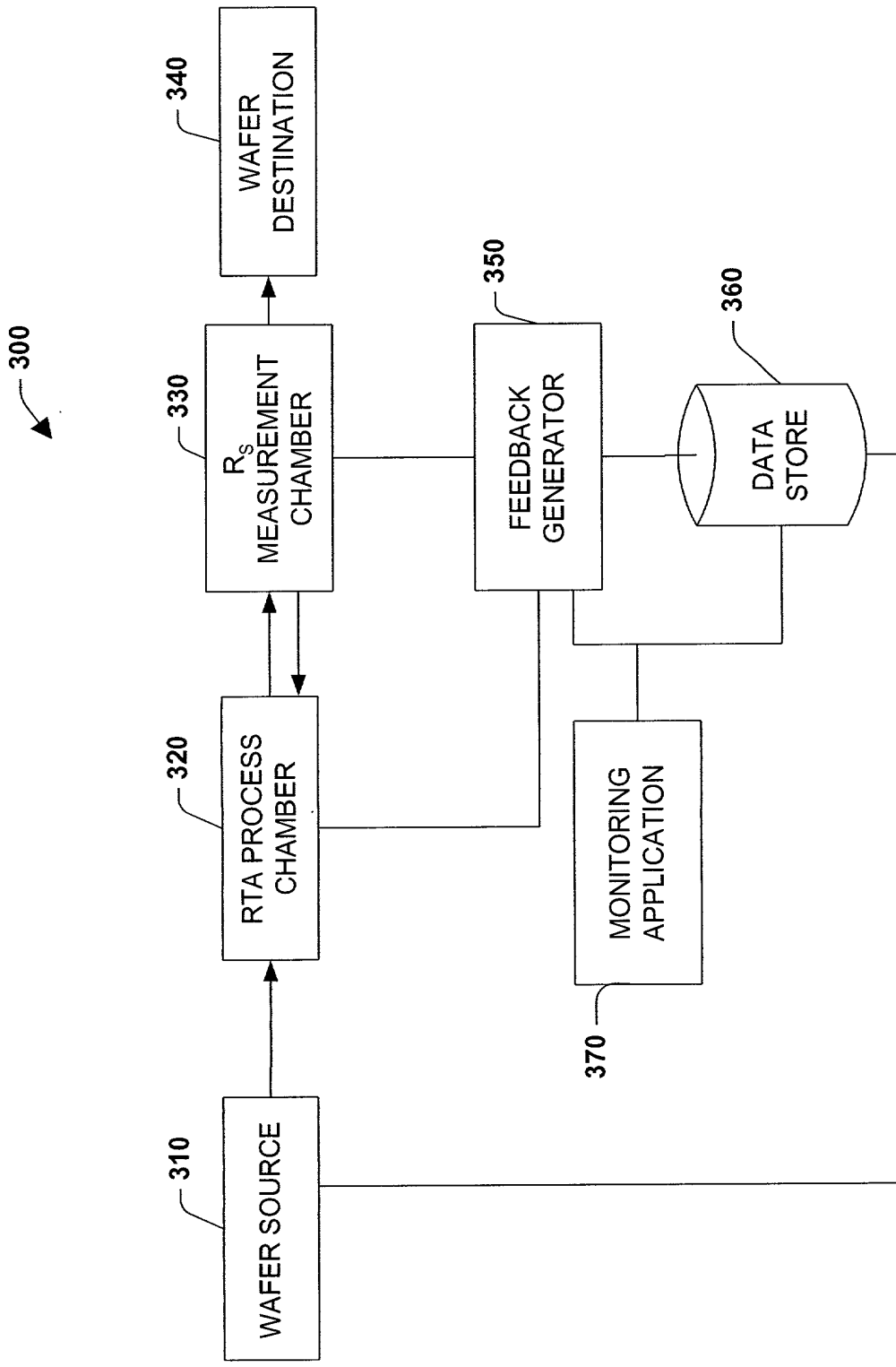


Fig. 2



**Fig. 3**

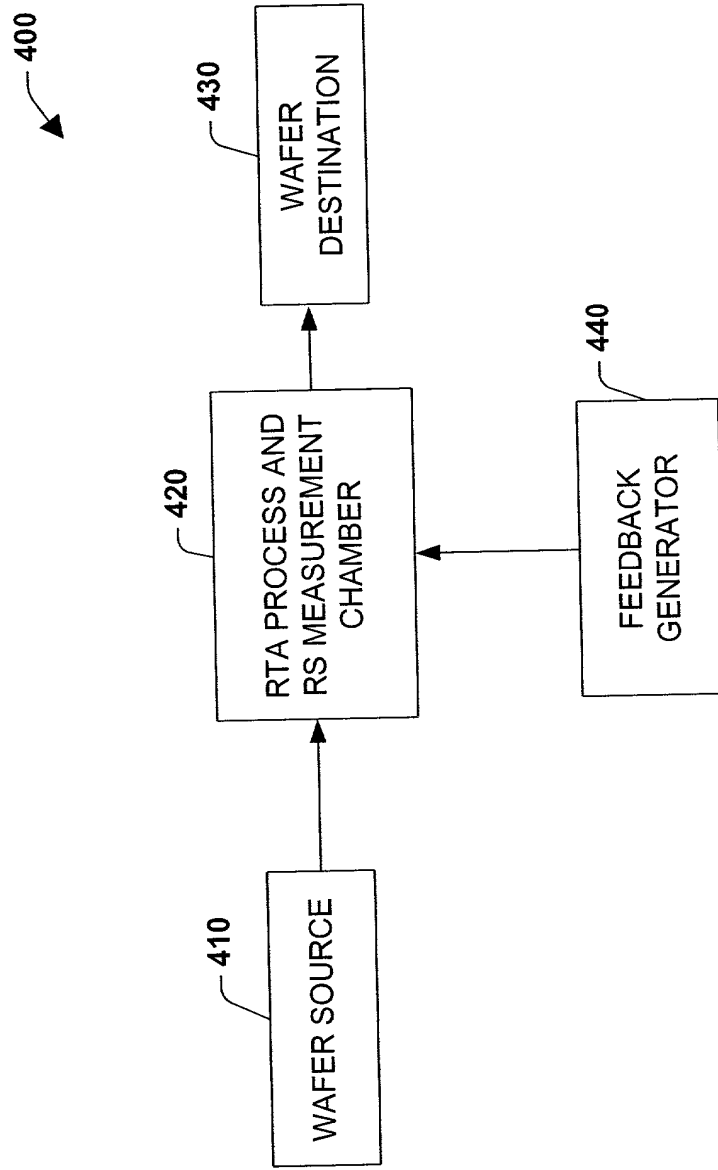


Fig. 4

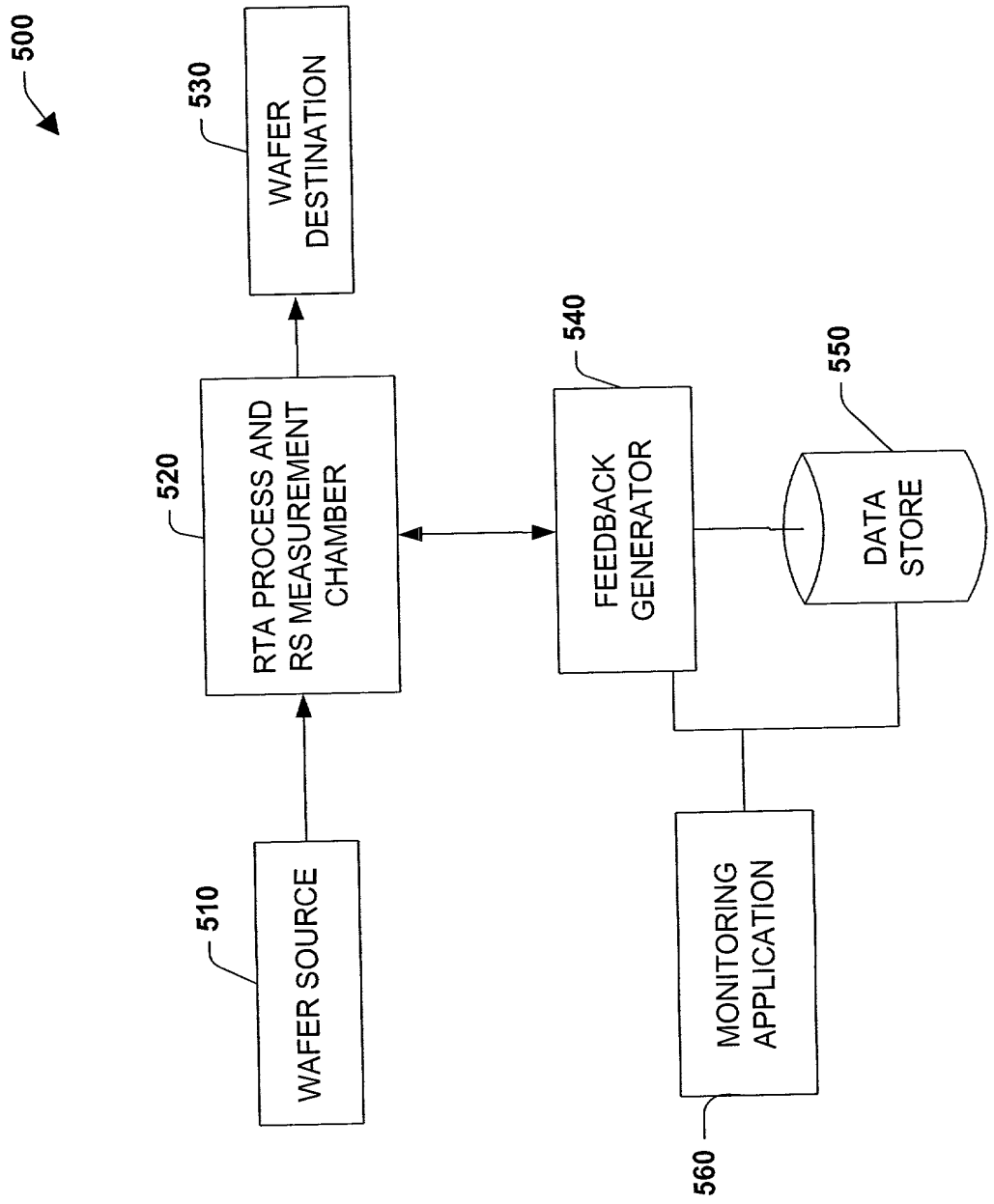


Fig. 5

FIG. 6 is a perspective view of a device 20. The device 20 includes a substrate 22 and a layer 24 disposed on the substrate 22. The layer 24 is a cross-hatched area. The device 20 is shown in a perspective view.

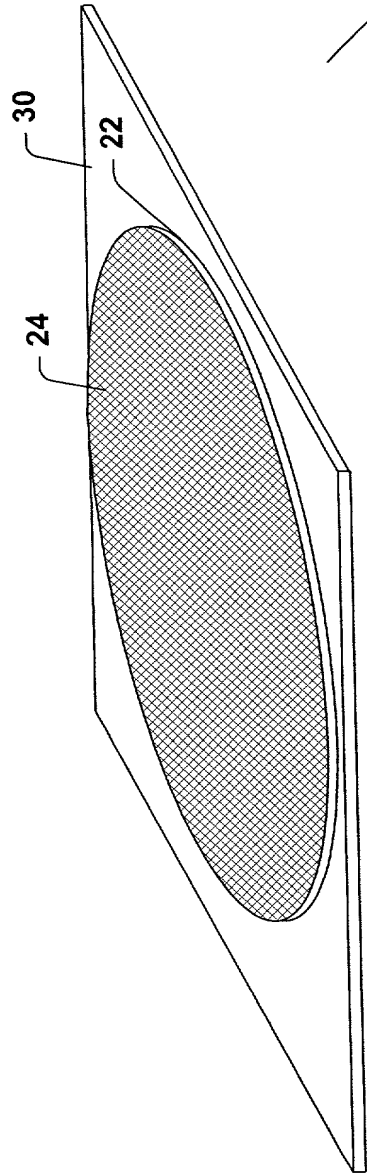


Fig. 6

	$X_1$	$X_2$	$X_3$	$X_4$	$X_5$	$X_6$	$X_7$	$X_8$	$X_9$	$X_{10}$	$X_{11}$	$X_{12}$
$Y_1$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_2$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_3$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_4$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_5$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_6$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_U$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_7$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_8$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_9$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_{10}$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_{11}$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$
$Y_{12}$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$	$T_A$

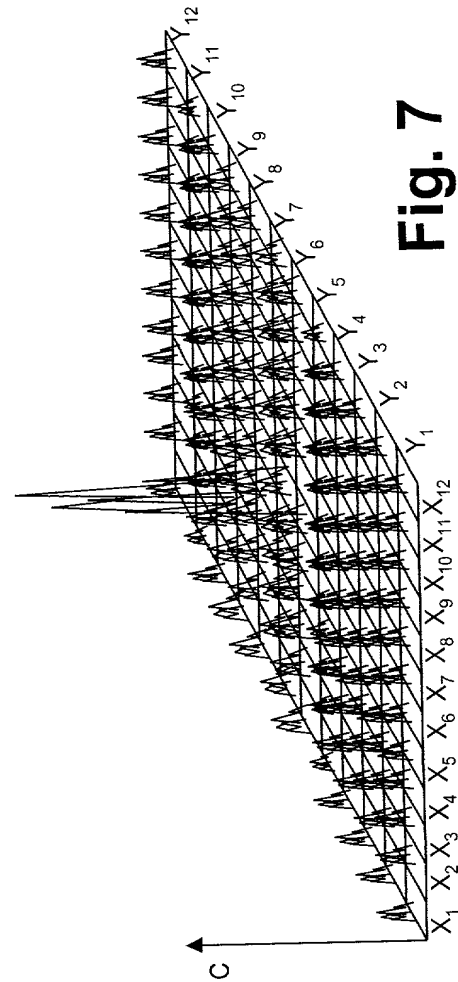


Fig. 7

Fig. 8

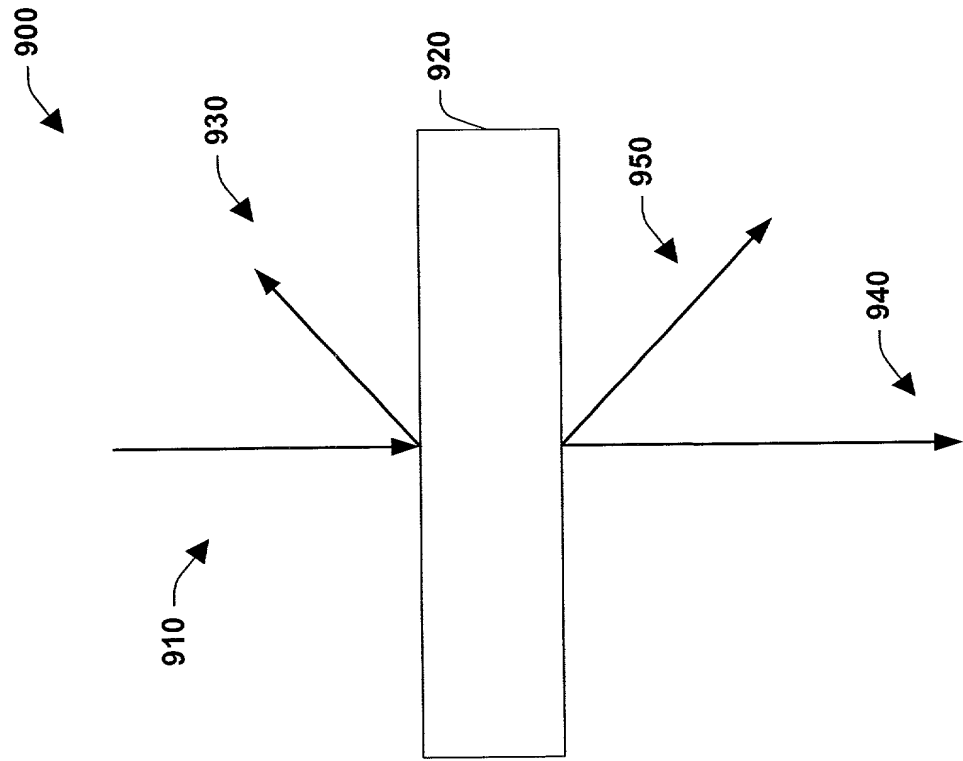


FIG. 9

FIG. 10 is a schematic diagram of a device 1000, which is a cross-sectional view of a device. The device 1000 includes a substrate 1010, a gate stack 1020, a gate electrode 1030, a gate insulator 1040, and a gate conductive layer 1050. The gate stack 1020 is formed on the substrate 1010. The gate electrode 1030 is formed on the gate stack 1020. The gate insulator 1040 is formed on the gate electrode 1030. The gate conductive layer 1050 is formed on the gate insulator 1040.

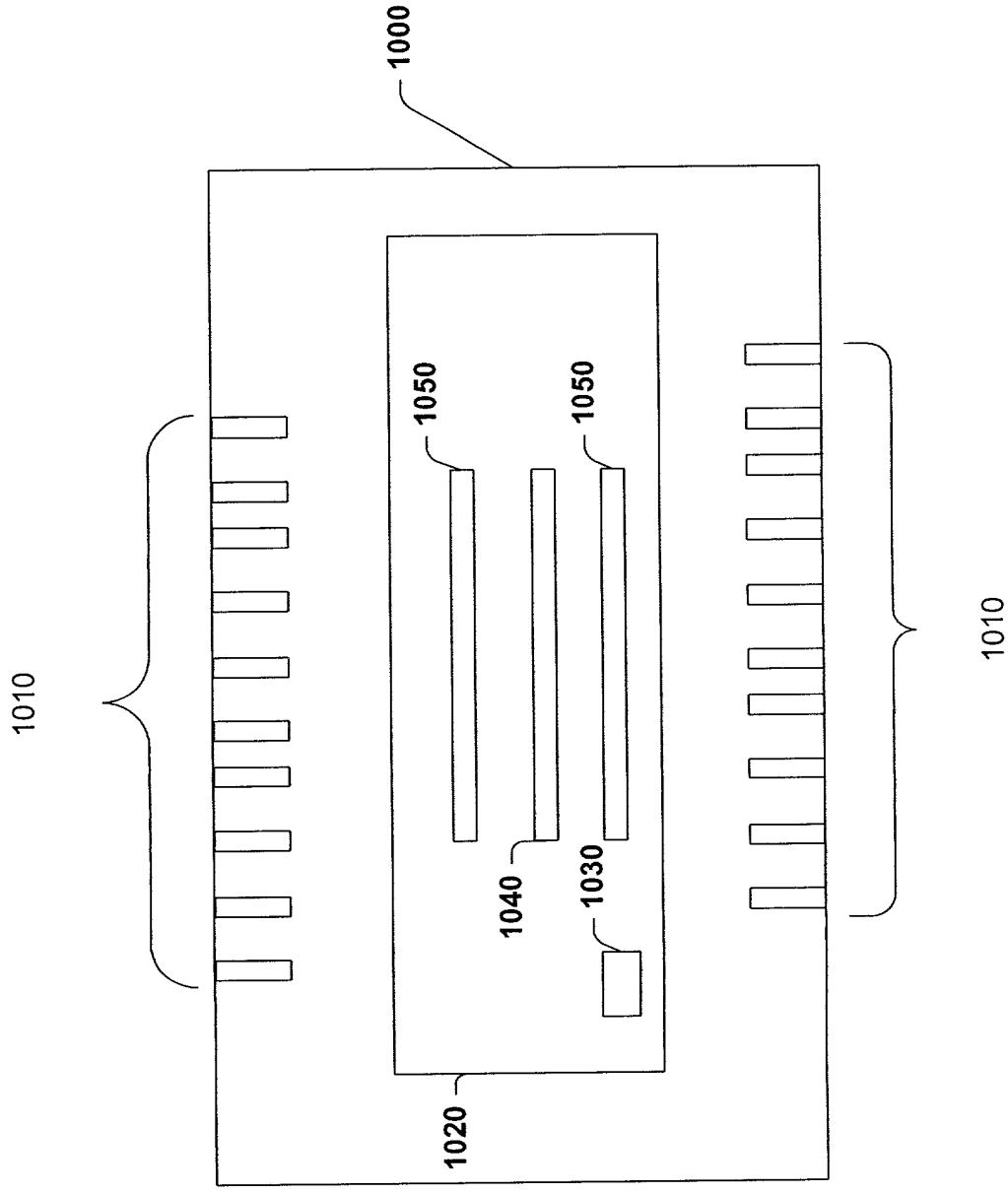


FIG. 10



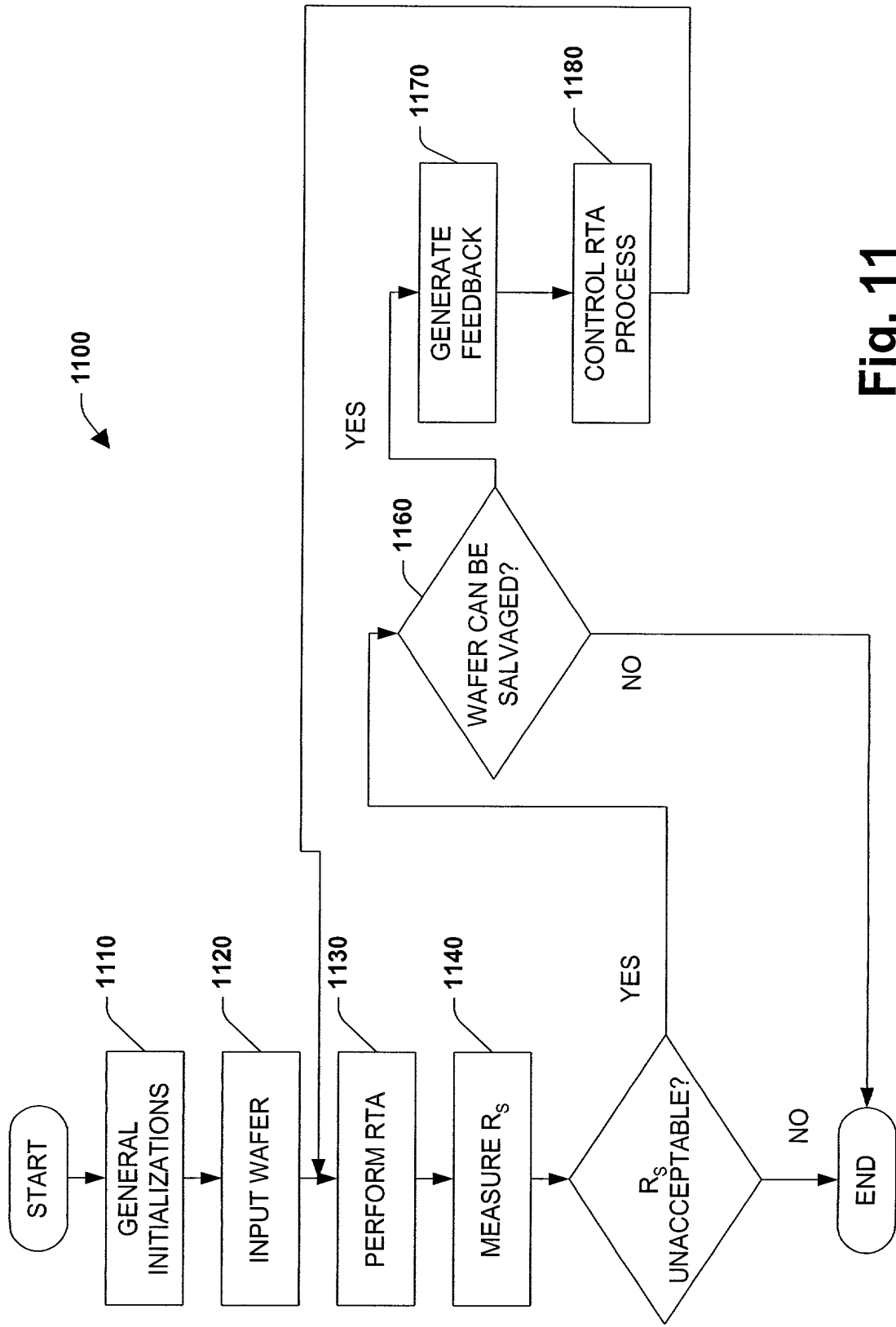


Fig. 11

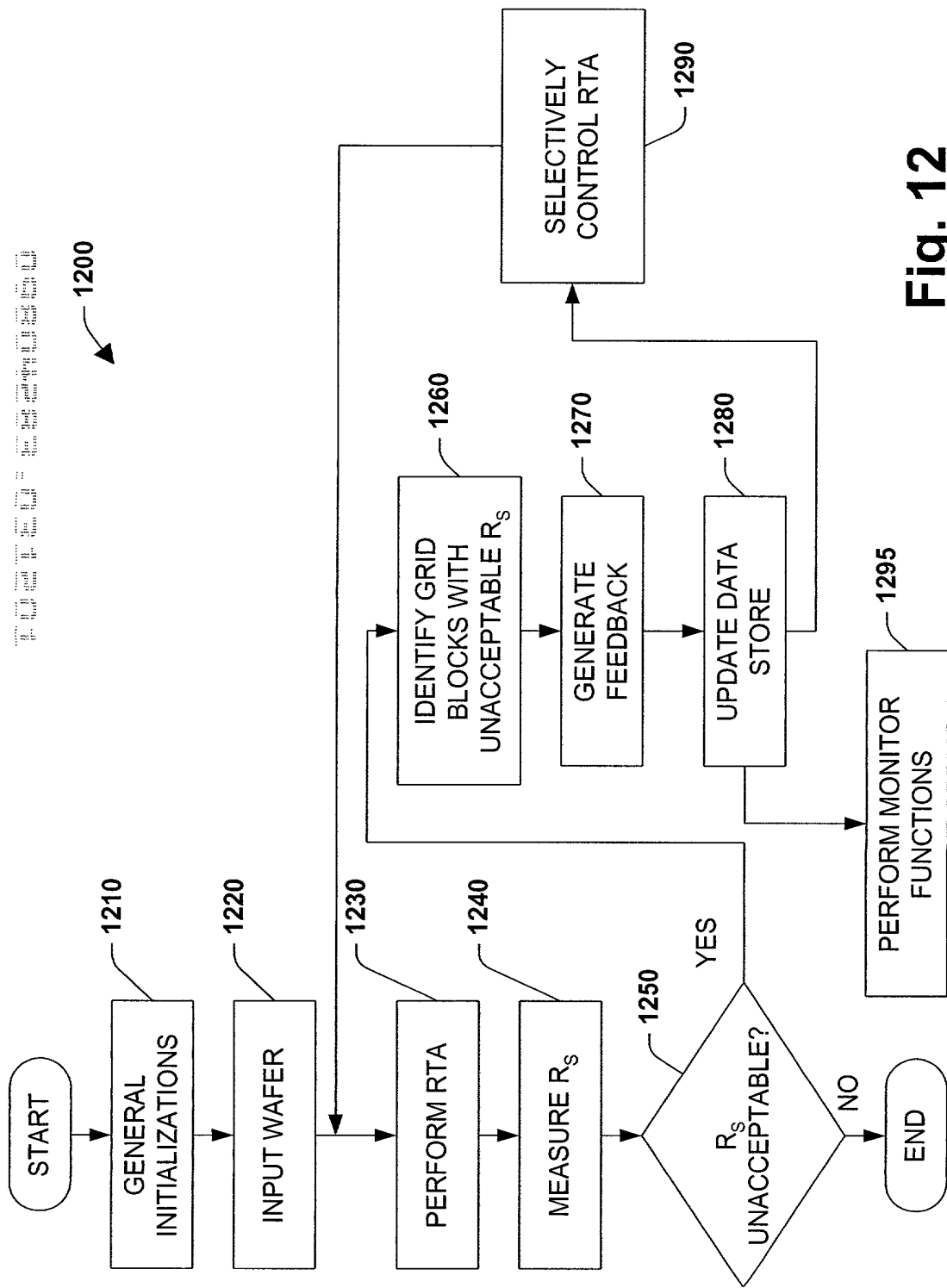


Fig. 12